PATENT APPLICATION

METHOD AND SYSTEM FOR ROUTE CONTROL REDUNDANCY FOR OPTICAL NETWORK SWITCHING APPLICATIONS

Inventors:

Krishna Kumar Ramadas, a citizen of the United States, residing at 20636 Craig Court, Cupertino, CA 95014; and

Srinivasa R. Tadimeti, a citizen of India, residing at 3276 Brittany Court, San Jose, CA 95135

METHOD AND SYSTEM FOR ROUTE CONTROL REDUNDANCY FOR OPTICAL NETWORK SWITCHING APPLICATIONS

5 BACKGROUND OF THE INVENTION

This present invention generally relates to techniques for optical switching. More particularly, the present invention provides a method and system for monitoring and/or controlling communication signals using out band connectivity. Merely by way of example, the invention is applied to a MEMS based switching system over a wide area

10 network for long haul communications. But it would be recognized that the invention could also be applied to other types of switching such as wave guides, electro-optic devices, holographic switches, bubble switches, liquid crystal switches, and many others for applications including metropolitan, access, and other networks.

Over the past years, digital telephone has progressed with a desire for

15 faster communication networks. In general, conventional analog voice telephone signals have been converted into digital signals. These signals can have transmission rates of 64,000 bits/second and greater in some applications. Other telephone circuits interleave these bit streams from 24 digitized phone lines into a single sequence of 1.5 Mbit/second, commonly called the T1 or DS1 rate. The T1 rate feeds into higher rates such as T2 and

20 T3. A T4 may also be used. Single mode fiber optics has also been used at much higher speeds of data transfer. Here, optical switching networks have also been improved. An example of such optical switching standard is called the Synchronous Optical Network (SONET), which is a switching standard designed for telecommunications to use transmission capacity more efficiently than the conventional digital telephone hierarchy,

25 which was noted above. SONET organizes data into 810-byte "frames" that include data on signal routing and designation as well as the signal itself. The frames can be switched individually without breaking the signal up into its components, but still require conventional switching devices.

Most of the conventional switching devices often require the need to

30 convert optical signals from a first source into electric signals for switching such optical signals over a communication network. Once the electric signals have been switched, they are converted back into optical signals for transmission over the network. As merely an example, a product called the SN 16000, BroadLeaf™ Network Operating System (NOS), made by Sycamore Networks, Inc. uses such electrical switching technique.

Other systems have been developed by Lucent Technologies, Inc., Ciena Corporation, and other companies. Numerous limitations exist with such conventional electrical switching technique. For example, such electrical switching often requires a lot of complex electronic devices, which make the device difficult to scale. Additionally, such electronic devices become prone to failure, thereby influencing reliability of the network. The switch is also slow and is only as fast as the electrical devices. Accordingly, techniques for switching optical signals using a purely optical technology have been proposed. Such technology can use a wave guide approach for switching optical signals. Unfortunately, such technology has been difficult to scale and to build commercial devices.

Other companies have also been attempting to develop technologies for switching a high number of signals in other ways such as high density mirror arrays, but have been generally unsuccessful. A major obstacle for such high density mirror arrays is limited control software and complex system architecture. Conventional control software and the like have been developed for optical-to-electrical-to-optical switches. Such conventional software has been effective for controlling electrical communication signals. Although effective for such electrical signals, they have limited applicability for optical communication signals and problems related thereto. Accordingly, such attempts have generally been unsuccessful.

From the above, it is seen that an improved way to manufacture a switching device is highly desirable.

SUMMARY OF THE INVENTION

According to the present invention, techniques including methods and systems for optical switching are provided. More particularly, the present invention provides a method and system for monitoring and/or controlling communication signals using out band connectivity. Merely by way of example, the invention is applied to a MEMS based switching system over a wide area network for long haul communications. But it would be recognized that the invention could also be applied to other types of switching such as wave-guides, electro-optic devices, holographic switches, bubble switches, liquid crystal switches, and many others for applications including metropolitan, access, and other networks.

In a specific embodiment, the invention provides an optical switching system. The system has an optical cross-connect, the optical cross connect having a

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plurality of mechanical switching devices. Each of the switching devices is capable of defecting a light beam from an input port to an output port. The system also has a communication interface bus coupled to the optical cross-connect; and a first routing module is coupled to the communication interface bus. The first routing module

5   comprises a route forwarding table. A second routing module is coupled to the communication interface bus. The second routing module is adapted to provide a redundant process for the first routing module. The second routing module is adapted to receive a copy of the route-forwarding table from the first routing module during a time period that the first routing module is active.

10   In an alternative specific embodiment, the invention provides an optical switching system having a redundant route control for out of band communication interface. The system has an in-band optical cross-connect having a plurality of mechanical switching devices. Each of the switching devices is capable of defecting a light beam from an input port to an output port in an in-band communication interface.

15   The system also has a communication interface bus coupled to the optical cross-connect; and a first routing module coupled to a first network connection for an out of band communication interface. The first routing module is coupled to the communication interface bus. A second routing module is coupled to a second network connection for an out of band communication interface. The second routing module is also coupled to the

20   communication interface bus, where the second routing module is adapted to provide a redundant process for the first routing module.

                Many benefits are achieved by way of the present invention over conventional techniques. In a specific embodiment, the present invention provides an easy way to make the present system more efficient during failure of one of the route

25   engine cards. Additionally, the present invention is modular which allows a system operator to repair selected cards or modules without interfering with the operation of the system. The invention can be implemented using conventional hardware and/or software technologies. In other aspects, the invention is generally compatible with other network systems that are based on standard network protocols such as Internet Protocol,

30   commonly known as IP. The present method and system are implemented in a purely optical based switch, which is scalable to switch a high density of optical signals. Preferably, the present invention provides for a system, which efficiently converts operation of one route engine card with another without undue delay or disruption, which is undesirable for carriers. Depending upon the embodiment, one or more of these

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benefits may be achieved. These and other benefits will be described in more throughout the present specification and more particularly below.

Various additional objects, features and advantages of the present invention can be more fully appreciated with reference to the detailed description and accompanying drawings that follow.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is simplified diagram of an optical switching network according to an embodiment of the present invention;

Fig. 1A is a simplified diagram of the present system in an alternative deployment embodiment;

Fig. 2 is a detailed diagram of an optical switching system according to an embodiment of the present invention;

Fig. 3 is a more detailed diagram of an optical switching system according to an embodiment of the present invention;

Fig. 4 is a more detailed block diagram of an optical switching system according to an alternative embodiment of the present invention;

Figs. 4A through 4H are more detailed diagrams of elements in the system according to embodiments of the present invention; and

Figs. 5 and 6 are simplified diagrams of alternative system diagrams for redundancy according to embodiments of the present invention

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

According to the present invention, techniques including methods and systems for optical switching are provided. More particularly, the present invention provides a method and system for monitoring and/or controlling communication signals using computer software and/or hardware. Merely by way of example, the invention is applied to a MEMS based switching system over a wide area network for long haul communications. But it would be recognized that the invention could also be applied to other types of switching such as wave guides, electro-optic devices, holographic switches, bubble switches, liquid crystal switches, and many others, for applications including metropolitan, access, and other networks.

Fig. 1 is simplified diagram 100 of an optical switching network according to an embodiment of the present invention. This diagram is merely an example, which

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should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. As shown, the diagram illustrates an optical network system 100 including a plurality of SONET rings or the like, which are shown by a cloud 101 configuration. Each of the SONET rings is

5   coupled to one or more network switching systems 103, 105, which are coupled to each other. The network switching systems can be coupled to long haul optical network system. In a specific embodiment, each of the systems switches an optical signal from one of the rings to another one of the rings, where the transmission path is substantially optical. That is, the signal is not converted into an electrical signal via an optoelectronic

10   device, which is coupled to an electrical switch that switches the signal. In the present embodiment, the transmission path is substantially optical. Further details of the switching system are provided below.

In a specific embodiment, the invention provides a system for bypassing traffic from the SONET networks, which can be congested, onto optical networks, as

15   shown in Fig. 1A. The traffic from the congested SONET rings from regional, national, local, interoffice, and others will be tapped off and transported across the country to the destination. The switches can be deployed at major hubs to add, drop, and transport traffic through the network. Shown below are typical examples of how the present switches may be configured to relieve the SONET traffic.

20   At least two reference models have been provided for the deployment of optical switches. In a preferred embodiment, the present system supports each of the models based on customer needs. The present deployment model (not shown) is a simplified physical implementation of the SONET node and how the present switch system connects to it. (Also not shown are the DWDM transport termination boxes,

25   which feed the de-multiplexed signals to the present systems). Alternatively, the present system can be coupled to nodes with DWDM terminating equipment. The system supports connection from remote and collocated routers through DWDM interfaces. For local router control it is often desirable to use a transponder to map wavelengths to a telephone network grid.

30   Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a combination of hardware and software. Alternatively, the above elements can be further

integrated in hardware or software or hardware and software or the like. The present system can also be deployed in other configurations, as well. It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

Fig. 2 is a detailed diagram of an optical switching system 200 according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. As shown, the switching system 110 includes a variety of features such as a switching apparatus 207. Apparatus 207 couples to incoming fiber bundles 213 through multiplexer/demultiplexer devices 211. In a preferred embodiment, the multiplexer/demultiplexer devices are DWDM devices, which receive signals from incoming fiber bundle 213 and separate such signals into channels 209, each representing a wavelength or the like. Apparatus 207 also couples to outgoing fiber bundles 215 through multiplexer/demultiplexer devices 217. In a preferred embodiment, the multiplexer/demultiplexer devices are DWDM devices, which receive channels representing wavelengths 219 from the apparatus and output such channels as outgoing optical signals.

A communication control device 205 couples to the apparatus. Such control device is overseen by a computing device 201, which includes a display. The computing device can be any suitable microprocessor based device. The computing device couples to display 202. Depending upon the embodiment, a variety of software processes can be incorporated into the computing device, which have been described throughout the present specification and more particularly below. Additionally, further details of the apparatus are also provided throughout the present specification and more particularly below.

Fig. 3 is a more detailed diagram of an optical switching system 300 according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. As shown, the system has a variety of elements including fiber interfaces, 305, which couple to cross-connect 302. Fiber interfaces 305 couple to multiplexers/demultiplexers, DWDM devices, 317, 307. Device 317 has input fiber bundle 341 and output fibers 315,

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which are numbered from 1 to n, representing integers for example. Device 307 has output fiber bundle 343 and output fibers 309, which are numbered from 1 to n. The data path through the interface devices and cross-connect correspond to light paths through the fiber interfaces, and the switching matrices. In a specific embodiment, the paths are

5   switched at configuration through user control or dynamically through multi-protocol latched switching (MPLS) signaling messages. In preferred embodiments, generally all data paths through the system have redundant configurations to support high system availability and avoid single points of failure. Other elements include a performance monitoring module 303 coupled to the interface and an alarm 301 coupled to the module.

10   Additionally, the system includes a packet extractor 323 coupled to the cross-connect 302 via line 337. A route control 319 is coupled to the packet extractor via line 321. Overseeing and controlling the system is control 327 coupled via line 325. Communication control 331 is coupled to control via line 329. The communication control 331 couples to network management modules via network interface 333.

15   As further shown, the system also has route control engine 334, which is external. The external route control engine couples to control and communication control. The external route control engine can be used to route IP packets to and from the switching device. The external route control engine often uses an external high-speed communication bus for fast and efficient transfer of information. In a preferred

20   embodiment, the external route control engine also has a backup, which will be described more fully below. Further details of networking and other interface devices are provided below.

Fig. 4 is a more detailed block diagram 400 of an optical switching system according to an alternative embodiment of the present invention. This diagram is merely

25   an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in this Fig. as the previous Fig. for cross-referencing purposes only. As shown, the system includes interface devices, such as a local area network 401, which couples to the routing engine control 319. The system also

30   includes a common system control bus 403, which couples to optical switch module 302 and alarm clock card 301. The control bus also couples to power system control 327. The system control bus also couples to shelf control card, which couples to fiber interface card 305 and couples to performance monitoring card 303 through shelf control bus 407.

The system control bus 409 couples to shelf control card, which also couples to fiber interface card 305 and performance monitoring card 303 through shelf control bus.

The system includes route control engine 319, which can be external or internal, as noted above. The external route control engine couples to control and communication control. The external route control engine can be used to route IP packets to and from the switching device. The external route control engine often uses an external high-speed communication bus for fast and efficient transfer of information. In a preferred embodiment, the external route control engine also has a backup, which will be described more fully below.

Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a combination of hardware and software. Alternatively, the above elements can be further integrated in hardware or software or hardware and software or the like. Further details of each of the elements in this diagram are provided throughout the specification and more particularly below.

Figs. 4A through 4H are more detailed diagrams of elements in the system according to embodiments of the present invention. These diagrams are merely examples, which should not unduly limit the scope of the claims herein. Each of the elements can be implemented using a combination of hardware and/or software. Such elements include: Routing Engine Card; Shelf Control Cards; Fiber Interface Cards; Switch Fabric; Packet Extraction Cards; Performance Monitoring card; Backplane; Alarm Clock Card; and Power Supply System. All of the above elements are preferably field replaceable. Additionally, the term "card" is not intended to describe any physical device but is merely used for illustrative purposes. A brief description of the elements is presented below.

Routing Engine Card

Referring to Fig. 4A, the system includes a Routing Engine Control (REC) card, which is the main system controller in a specific embodiment. The REC card manages configuration of the system, interfaces and oversees most if not all element management systems, processes IP control messages, and administers control and data buses in the system. REC cards are installed in a 1+1 redundant configuration with

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mastership logic used to determine the active and standby states of the switches. Functions of the REC are to provide the control interface, manage the system resources, and process IP control messages to and from a Packet Extraction Card (PEC), which will be described in more detail below.

5 In a specific embodiment, the REC includes a control processor 402, control bus communication 413, packet interchange bus 412, mastership control 404, and memory systems 405, 406. The control processor can be any suitable micro processing device such as an Intel Pentium based controller manufactured by Intel Corporation of Santa Clara, California, which includes boot logic and reset logic 403, a clock oscillator,

10 LED indicators, and other features. As shown, the REC card includes a system control bus interface 410, which can be a high-speed serial 1394 bus or any other suitable device. The control bus interfaces to the shelf controllers, the optical switch matrix, alarm control, and the power system control for configuration, monitoring, and administration functions.

15 As shown, the REC has a serial port 408 to support a Crafts interface. The serial port can be any suitable port such as an RS232 port that is auto-sensing for port speed. The REC also has a plurality of local area networking (i.e., Ethernet) ports 409 to support LAN access. Such LAN ports interface to network management and additional future network elements. A packet interchange bus 411 communicates between the PEC

20 and the REC. The package interchange bus is based on the compact PCI bus architecture. The PCI common bus will be for configuration and management in addition to supporting configuration and management. The REC card includes support storage of selected system and network configuration to hard-disk media, which is a local disk system 407 located on the REC. In a specific embodiment, the present system allows the REC to

25 process up to 25,000 messages per second and greater.

Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a

30 combination of hardware and software. Alternatively, the above elements can be further integrated in hardware or software or hardware and software or the like.

Shelf Control Card

Referring to Fig. 4B, a shelf control card 420 is illustrated. The shelf control card controls configuration and management of the Fiber Interface Cards (FICs) and Performance Monitoring Cards (PMCs), which are described in more detail below. The shelf control card also communicates with the system controller for overall system

5   control functions. The card is based upon a suitable processor such as an Intel-based processor designs, but can be others. Preferably, the cards support communication paths through the system. Each of these cards is installed in redundant or non-redundant configuration on a per shelf basis. 1+1 redundancy is the configuration of choice for the system.

10   In a specific embodiment, the control card 420 is composed of elements that support the general processing environment. The card has a processor 421, memory 424, 425, boot code and reset circuitry 422, and master control 423. Additionally, master control 423 determines which card is the active and standby controllers. The shelf controllers communicate through Compact PCI bus 428 to the FICs and the PMCs. The

15   PCI bus is designed in a master/slave architecture to provide efficient communication. Each shelf card will be memory mapped to allow information to be exchanged between the system communication control (SCC) 427 and other cards installed on the shelf. The shelf card also has serial interface 426, which can be a local serial port.

Although the above has been described in terms of specific system

20   hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a combination of hardware and software. Alternatively, the above elements can be further integrated in hardware or software or hardware and software or the like.

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Fiber Interface Card

Referring to Fig. 4C, a fiber interface card 440 is illustrated. The fiber interface card terminates fibers. In a specific embodiment, forty-eight fibers can be terminated, although there may be more or less. The fibers can be divided equally

30   between input and output. The input fibers are first sent to an array of twenty-four one by two (i.e., 1 X 2) switches. Each of such switches selects an input to the switch matrix between the incoming signal and a signal from a calibration source. The switch is synchronized with the signal coming from the calibration laser source, which prevents the calibration laser source signal and the incoming high speed optical signal from

propagating on the same fiber. The FIC also has an electrical control for the one by two switches. Each of the switches has control, which is registered. The registers are visible to the control processor over a PCI type of back plane bus.

In a specific embodiment, the calibration laser source is an 830nm laser with a mode harmonizing fiber, which harmonizes all the modes within the fiber. Such fiber is spliced with a 1 X 24 coupler. Each of the 24 outputs of the coupler transfers to a one by one (i.e., 1 X 1) on-off fiber-optic switch. Such one by one switch prevents one calibration beam spilling on to the other and cause cross-talk during calibration. The fiber carrying the signal then couples to a special coupler which splits the incoming signal into three parts with a predetermined ratio, e.g., 98:1:1. The two 1% legs transfer to an optical monitoring process and to the InGaAs photodiode + Amplifier array for "insertion loss" and "loss of signal" monitoring. The photodiode and amplifier convert the optical signal into an analog signal, which converts to digital using a digital to analog converter. The digital signal can be used with an alarm, which can also be a digital TTL type output from the InGaAs photodiode. The SOH optical monitoring is connected into a pair of 12 fiber connectors, where a signal is taken from the FIC to a separate card for Optical SOH monitoring.

The FIC also selects between an active and standby switch matrix. Here, the signal is derived from the FIC to a switch, which selects between an active and standby switch matrix. This switch is in an integrated package of 24 switches. The fiber coming out of the common switch port is taken to two separate pairs of 12 fiber connectors. While one pair is for the active switch matrix, the other is for the standby. On the outgoing fiber side, fibers are received from the active and standby switch matrices and then input into an array of 24 two by one switches. The common fiber is then spliced with a 99:1 coupler. This coupler is arranged in an array of 24. The outputs go to a 24:1 combiner and then on to a silicon photodiode. The 99% split is then sent to a coupler, which splits the signal three ways (98:1:1). One of the 1% splits goes to the InGaAs PD, which monitors "Insertion Loss" and "Loss of Signal". The other 1% split goes to the pair of 12 fiber connectors and then on to the SOH monitoring card. The 98% split is sent to the outside world. This 2x1 will switch the optical transport between the backup switch matrix and the active switch matrix card. The card will have some electronics circuitry to drive the 2x1 switch and the fiber interface chips. Fiber redundancy is achieved by simply changing the cross connect configuration.

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The fiber termination card taps individual fiber lines and extracts sample signals from each to monitor optical signal level and maybe other optical signal integrity signals. The sample signals or tap information is sent to the switch fabric. The back plane supports a limited number of fiber tap lines. The line card has special circuitry to select a smaller number of tap signals that will be placed into the back plane bus.

In a specific embodiment, the fiber path through the system can be diagnosable. Fiber termination card is a possible location to host the logic to insert and to detect test patterns. The insertion and detection mechanism on the fiber termination card together with the cross connect reconfiguration can help diagnose the entire optics path within the system. This fiber termination cards will work with the reference wavelength card to fully support performance monitoring requirements of the input optical signals. As shown, the FIC card has components to terminate the input fibers. The components include 1x2 Switches (input), taps for SOH & Power Level (e.g., input to 98%, 1%,1% output), 1x2 switches (output), a Calibration Source at 830nm, 1x1 switch (e.g., 0.4db loss, 2-3ms), a 1X24 coupler, a pair of 12 Fiber connectors for SOH monitoring, InGaAs (LW) PD's + Amplifiers + Reference voltage source for in-line power monitoring, an electrical Mux as a possible interface before Analog to Digital Converters and others. The FIC also has components to terminate output fibers. Such components include a Silicon PD with Pre-Amplifier, 1 to 2 couplers 99% and 1%, 1 to 3 taps for SOH & Power level (IL), 1x2 standby switches to select incoming signal between active and standby, 24 to 1 coupler, a pair of 12 Fiber connectors for SOH monitoring, four InGaAs (LW) PD's + Amplifiers + Reference voltage source for in-line power monitoring, an electrical Mux as a possible interface before Analog to Digital Converters, and others. Other elements include two connector pairs (1 for input and 1 for output) each connector has a plurality fibers. The other elements include connector pairs for Active and Standby Switches, and Connector pairs for fibers from Active and Standby switches. These and other elements are described in more detail below.

In a specific embodiment, the FIC has a fiber interface controller. That is, each shelf on the bay has it's own controller for the fibers coming in on it's shelf. The system controller switches each of the fibers on the shelf to main or the standby switching element. The FIC also has low cost + low frequency array of 48 photo-detectors. These convert the 1% split-off from the incoming signal to electrical signals, amplify them if necessary, compare them against a known threshold and flag the LOL signal if appropriate. Also the card will digitize the voltage corresponding to the input optical

power and pass it along over the data bus to the system controller. The system controller can extract the optical power info through the set algorithm from the digitized signal. The FIC also has on it a special optical module which takes an array of X fibers ($X \leq 48$) and using a two different taps converts an incoming light signal into three output signals of

5   power levels: 98%, 1% and 1%.

Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a

10   combination of hardware and software. Alternatively, the above elements can be further integrated in hardware or software or hardware and software or the like. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

Optical Switch Matrix

15   Referring to Fig. 4D, the system has an optical switch matrix that contains the switching fabric, digital control, analog control, and calibration circuitry to support the function of the switch. This module is a self-contained unit that is under the control of the REC to perform switching functions between optical input and output ports. The switch matrix digital control supports communication control from the REC, control of

20   analog interfaces, calibration functions, and monitoring of the switch integrity. The electronic circuitry is visible to the control processor card, perhaps, through a PCI type of back plane bus. A redundant switch matrix slot is provided to support field replacement. Electrical lines in the back plane indicate to the fiber interface cards the current active fabric card. Switchover is coordinated responsibility with the fiber interface cards.

25   Switch matrix diagnostics support isolating failures in the switching cells in a destructive manner. Self-test modes allow the entire switch fabric to be substantially free from defects. This may require external equipment to fully test data paths.

In a specific embodiment, the switch includes a switch fabric control to operate, monitor, and control each of the mirrors. The control uses analog control signals

30   to control each of the mirrors. In a specific embodiment, the matrix includes 513 mirrors in each 256X256 switch. Each mirror has at least 2 axis controls, which relate to 1024 control signals. Some of the mirrors may share a single analog control line or bus, which may be bi-directional so it can be written to and read from. Such bi-directional bus

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allows for a determination of mirror position. Each of the control signals is addressed and selectable. Each mirror has a read/write (R/W) select for the analog control signal. Other features include digital to analog (DA) and analog to digital (AD) converters. An auto-sense and auto-correct feedback control circuitry corrects for any wobble or oscillation in the mirrors. Switch matrix diagnostics support isolating failures in the switching cells in a destructive manner. These and other features are included in the mirror matrix design.

Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a combination of hardware and software. Alternatively, the above elements can be further integrated in hardware or software or hardware and software or the like. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

Packet Extraction Card

Referring to Fig. 4E, a packet extraction card 460 is illustrated. In a specific embodiment, optical signals from a selected number of fiber interfaces may be carried to the Packet Extraction Card (PEC). The Packet Extraction Card terminates signals directly from the switch matrix. The Packet Extraction Card extracts the SONET DCC channel from the optical stream. This card supports OC-192 and OC-48 and others. Support for higher speed interfaces such as OC-768 is also included. The extracted DCC payload is diverted to the Routing Engine Card as IP packets over the Packet Exchange. It is assumed that the wavelengths are carrying POS payload on the control streams. A signal extraction card may have more intelligence than the fiber interface cards and can have a small capacity general purpose CPU. A role of such a CPU may be to perform packet extractions and injection and to avoid terminating multiple SONET streams at the control processor. The main circuitry of the PEC supports the termination of the SONET signals, clock recovery, and extraction of the DCC channel. A control processor builds messages to and from the Routing Engine Card.

Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a combination of hardware and software. Alternatively, the above elements can be further

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integrated in hardware or software or hardware and software or the like. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

Performance Monitoring Card

Referring to Fig. 4F, a performance monitoring card 470 is illustrated. In a specific embodiment, performance monitoring of the optical signals is accomplished though using distributed and centralized circuitry. Each of the fiber termination cards supports checking signal levels through an optical line module. Centralized testing is supported on the tapped signals from the fiber interface cards. This is a central resource card that support dynamic checking of all 4096 fibers. An array of detectors for monitoring purposes from the Optical IC for termination/ DC optical power measurement purposes are included.

In a specific embodiment, methods according to an embodiment of the present invention may be outlined as follows.

    a) Estimated BER. The PMC measures bit error rate (BER) on an on-going shared basis. The PMC is coupled with the optical signal to noise ratio (OSNR) and power measurement at the ingress and egress of the optical signal from the switch.

    b) Optical SNR. The PMC measures signal to noise ratio (SNR) data on the system on an on-going shared basis using selected circuits, which are commercially available. As merely an example, equipment manufacturers like Tektronix or Agilent manufacture such circuits. Q-factor for the laser can be extracted from this data.

    c) Electrical SNR. The PMC measures electrical SNR on the signaling channel. Preferably, it is only for the signaling channel.

    d) Chromatic Dispersion. Chromatic dispersion will be measured. It is not required to measure this on an on-going basis but can be measured on an on-going basis.

    e) Polarization Mode Dispersion. Polarization Mode dispersion will be measured. It is not required to measure this on an on-going basis but can be measured on an on-going basis.

f) Wavelength registration. The present system should not be wavelength sensitive in preferred embodiments and there for wavelength registration may not be measured.

g) Wavelength Drift. The present system should not be wavelength sensitive. Accordingly, drift will not be monitored in some embodiments.

h) Cross-talk. The present system will measure switch cross-talk. Wavelength cross-talk may or may not be measured. Switch cross-talk is measured by comparing input vs output OSNR + optical power level comparison.

i) Optical Power transients. Optical power transients will be monitored. Such transients occur due to laser operation. Fluctuation in power, if any, at the output ports will be monitored. Such fluctuations can be due to a variety of reasons, such as, but not limited to wobbling of the mirrors. Such power fluctuations will be compared against the input power.

j) Insertion loss. This will be measured on a constant basis.

k) Jitter. Jitter will be measured during troubleshooting of the system using an oscilloscope coupled to the system.

l) Optical Power Level. This is measured on a constant basis or variable basis.

m) Bit Rate: This is measured for control channel only, but can also be measured at other points.

In a specific embodiment, the monitoring card also couples to a variety of external measurement tools. Such tools monitor functions such as BER using external equipment, CRC payload, and CRC header, and the like. The card will support short and long-term integrations of test cycles. This allows thresholds to be set for long-term-integration of alarm conditions that require automatic or manual intervention. All alarms and counters will be available to the element manager. The Performance monitoring card is configured and monitored via the Shelf Control Bus.

Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a

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combination of hardware and software. Alternatively, the above elements can be further integrated in hardware or software or hardware and software or the like. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

5   Alarm Clock Card

Referring to Fig. 4G, an alarm control card 480 is illustrated. The card includes various circuitry used to communicate to the central office the standard alarm indicators and provide system timing. The card is primarily composed of switches, relays, and PLL clocking circuit. The card conforms to Bellcore standards, as desirable.

10   This card contains a general controller that will process commands that indicate whether to set or release relays indicating alarm conditions and clearing of alarm conditions. The system timing requirements will be based on extracting clocking from external inputs, or BITs clock, or internal timing sources. Internal sources will be through from terminated SONET signals. The timing circuitry will phase-lock to the input provided for

15   synchronously running the system to a Stratum 3 clock source.

Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a

20   combination of hardware and software. Alternatively, the above elements can be further integrated in hardware or software or hardware and software or the like. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

        Power System and Control

25   Referring to Fig. 4H, a power system 490 is illustrated. The power system for the switch system is a redundant design to insure high-availability. The power systems are designed for –48VDC and 220VAC input voltages. Components of the power system include a (1) power supply controller, (2) power supply modules, and (3) the power chassis. One power system is used per bay but can also include more than one power

30   supply. Power consumption at each node should not exceed 1000W maximum. Power control and redundancy are managed on a per bay basis. Control circuitry support communication paths to the system controller (REC), load sharing, input voltage monitoring, and failure reporting. The communication path to the system controller is done through the system control bus. The cards will contain sensing circuitry for the input

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power to detect brown-out conditions. The power system provides +5VDC, -5VDC, +12VDC, -12VDC to the electrical backplane. Special voltage inputs to support the switch matrix may be required. The power system for the switch matrix card may also include an uninterrupted power supply (UPS) to keep power applied to the switch matrix

5   system to support power failure conditions.

The present system also includes an electrical backplane. The back plane supports the power to the cards, system control bus, shelf control buses, and the packet exchange bus. A desire is to have shelf busses be designed the same for the fiber interface shelves. These buses will also provide grounded pins for card slot recognition

10 to support addressing each card. There will be at least two different backplanes to support the fiber interface shelves and the controller shelf. The shelf control bus and the packet exchange bus will be based on the compact PCI architecture. This architecture supports hot swap capability which is required for the system. The backplanes support redundant buses to reduce single points of failure.

15 Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a combination of hardware and software. Alternatively, the above elements can be further

20 integrated in hardware or software or hardware and software or the like. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

Figs. 5 and 6 are simplified diagrams of alternative system diagrams for redundancy according to embodiments of the present invention. As shown, the system diagram 500 includes a variety of features such as network 501. The network can be a

25 world wide area (or wide area) network or other forms of networks. The network is coupled to a router 503. The router couples to hub 505, which couples to a primary REC and a backup REC. The backup REC is generally not in an active or functional state during operation of the primary REC. Each REC couples to a high speed bus 511, which couples to cross-connect 513. The REC has similar features as the REC described above

30 but can also include others. The REC generally has a high speed memory device, such as a DRAM or SRAM, for maintaining route forwarding information.

Referring to Fig. 6, primary routing engine couples through path 617 to hub or other switching device and backup routing engine couples through path 619 to hub or other switching device. The primary routing engine 607 has a forwarding table 601

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and route database 609. As noted, the route forwarding table is often implemented in a high speed memory device, such as DRAM, SRAM, or the like. The route database is often provided in a hard disk or other suitable memory with sufficient capacity. As merely an example, route forwarding information includes the following information (Table 1):

Destination IP Address	Mask	Gateway	Interface
10.0.128.63	255.255.255.255	0.0.0.0	Ethernet0
192.168.0.0	255.255.128.0	10.0.128.254	Ethernet0
0.0.0.0	10.0.128.1	0.0.0.0	Ethernet1

Table 1: Route Forwarding Information

As shown are selected parameters that define the forwarding table. As also show is a destination IP address, which can be a 32-bit number. Here, the 32-bit number is composed of four-8-bit numbers. Each of the eight bit numbers can represent a number from 0 to 255. An example of such a 32-bit number is 191.5.23.32. This 32 bit number can mask the last number by inserting "0," where the final IP address is 191.5.23.32, where the 0 is used as a mask to determine any possible configuration for the address on the last eight bit number. The mask indication could also be used to provide other combinations such as 16-bit or 22-bit. The table also lists the "gateway," which is the next hop. Also shown is the "interface" which is the type of port used to send the IP packets. Such medium includes Ethernet and other types of interfaces.

The backup routing engine 601 also includes route database 603 and route forwarding table 605. As the route forwarding table in the primary route engine is being formed, the route forwarding table in the backup is also formed, but is not active. Alternatively, portions of the route forwarding table are the same in each of the route engines. The portions can be the entire route forwarding table or a portion (e.g., only part) of the route forwarding table for efficiency purposes.

In operation, the backup REC serves as a backup for the primary REC. When the primary REC goes down, the following processes occur. The address associated with the primary routing engine transfers to the backup engine. In a specific embodiment, the primary IP address 621 is transferred over 615 to the backup engine 623 such that the back up engine receives and transfers information from the backup engine as

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if it was the primary engine. As noted, the forwarding table is generally the same 613 for each of the routing engines. Accordingly, the backup operation can be performed in an efficient manner without undue delay. Once the backup REC is being used, the process builds the route database 603 for the backup REC.

5   Although the above has been described in terms of specific system hardware features, it would be recognized that there could be many alternatives, variations, and modifications. For example, any of the above elements can be separated or combined. Alternatively, some of the elements can be implemented in software or a combination of hardware and software. Alternatively, the above elements can be further

10   integrated in hardware or software or hardware and software or the like. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

          The system is merely provided to show an example of a way of implementing the present invention. It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various

15   modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.